AMENDMENTS TO THE CLAIMS:

1-22. (Canceled)

23. (Currently amended) A test method for verifying fabrication of transistors in an integrated circuit, said test method comprising:

providing a ring oscillator on a die under test during fabrication of said die, said ring oscillator including a plurality of delaying stages connected in cascade, and a like plurality of transfer gates, each transfer gate coupled to ~~each~~ a corresponding one of said plurality of delaying stages, each of said transfer gates including a pair of transistors of ~~the~~ first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by the same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die;

measuring a first period of said ring oscillator by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF;

measuring a second period of said ring oscillator by operating said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second conductivity type of each of said transfer gates are ON;

measuring a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

24. (Currently amended) The test method as claimed in claim 23, wherein ~~said step of~~ analyzing includes: ~~the steps of:~~

comparing said first period with a first preselected specification;

comparing said second period with a second preselected specification; and

comparing said third period with a third preselected specification.

25. (Original) The test method as claimed in claim 23, wherein the total number of said plurality of delaying stages is odd, wherein each of said delaying stages includes a CMOS inverter, and wherein said pair of transistors of each transfer gate are p-channel and n-channel transistors, respectively.

26. (Original) The test method as claimed in claim 23, wherein said ring oscillator includes an NAND input stage, wherein the total number of said plurality of delaying stages is even, and wherein each of said delaying stages includes a CMOS inverter, and wherein said

first and second conductivity type transistors are p-channel and n-channel transistors, respectively.

27. (Currently amended) A test apparatus for verifying fabrication of transistors in an integrated circuit, said test apparatus comprising:

a ring oscillator provided on a die under test during fabrication of said die, said ring oscillator including a plurality of delaying stages connected in cascade, and a like plurality of transfer gates, each transfer gate coupled to ~~each~~ a corresponding one of said plurality of delaying stages, each of said transfer gates including a pair of transistors of ~~the~~ first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by the same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die;

circuitry operable for measuring

a first period of said ring oscillator by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF,

a second period of said ring oscillator by operating said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second

conductivity type of each of said transfer gates are ON, and

a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

circuitry operable for analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

28. (Original) The test apparatus as claimed in claim 27, wherein said circuitry operable for analyzing includes:

circuitry operable for comparing said first period with a first preselected specification;

circuitry operable for comparing said second period with a second preselected specification; and

circuitry operable for comparing said third period with a third preselected specification.

29. (Currently amended) A computer program product embodied in a storage media, the computer program product including a program of instructions for performing a test method, the test method comprising:

measuring a first period of a ring oscillator for a die under test,

wherein said ring oscillator is provided on said die during fabrication of said die, said

ring oscillator including a plurality of delaying stages connected in cascade, and a like plurality of transfer gates, each transfer gate coupled to ~~each~~ a corresponding one of said plurality of delaying stages, each of said transfer gates including a pair of transistors of ~~the~~ first and second conductivity types connected in parallel, said transistors of the first conductivity type and said transistors of the second conductivity type being fabricated by the same processes as transistors of the first conductivity type and transistors of the second conductivity type constituting an integrated circuit on said die,

said ~~step of~~ measuring said first period being carried out by operating said ring oscillator to provide a first oscillator output signal during a first mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are OFF;

measuring a second period of said ring oscillator by operating said ring oscillator to provide a second oscillator output signal during a second mode when said transistors of the first conductivity type of each of said transfer gates are OFF and said transistors of the second conductivity type of each of said transfer gates are ON;

measuring a third period of said ring oscillator by operating said ring oscillator to provide a third oscillator output signal during a third mode when said transistors of the first conductivity type of each of said transfer gates are ON and said transistors of the second conductivity type of each of said transfer gates are ON; and

analyzing said first, second and third periods for decision making on whether said integrated circuit on said die meets preselected specification.

30. (Currently amended) The computer program product as claimed in claim 29, wherein said ~~step of~~ analyzing includes:

comparing said first period with a first preselected specification;

comparing said second period with a second preselected specification; and

comparing said third period with a third preselected specification.